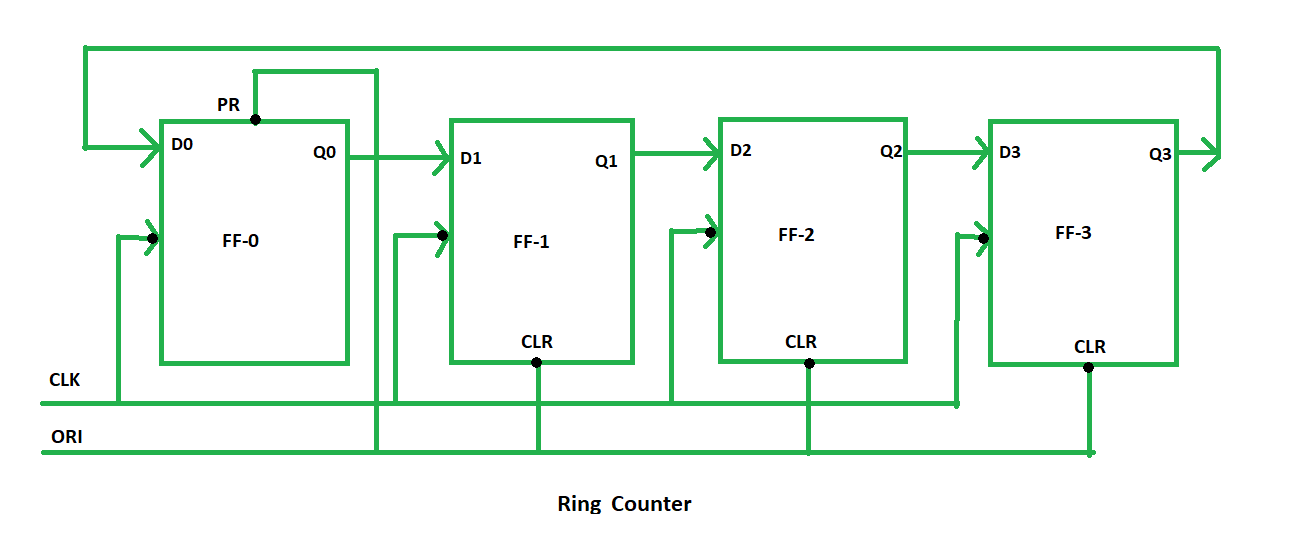
**COUNTERS & TIMERS**

1. Design & explain working of:
2. 4-bit Ring counter

Ans: A ring counter is a typical application of the Shift register. The ring counter is almost the same as the shift counter. The only change is that the output of the last flip-flop is connected to the input of the first flip-flop in the case of the ring counter but in the case of the shift register it is taken as output. Except for this, all the other things are the same.

No. of states in Ring counter = No. of flip-flop used



A grid of numbers and symbols

Description automatically generated with medium confidence PR = 0, Q = 1

CLR = 0, Q = 0

4 states are:

1 0 0 0

0 1 0 0

0 0 1 0

0 0 0 1

**Types of Ring Counter:** There are two types of Ring Counter:

1. **Straight Ring Counter:** It is also known as One hot Counter. In this counter, the output of the last flip-flop is connected to the input of the first flip-flop. The main point of this Counter is that it circulates a single one (or zero) bit around the ring.

A diagram of a computer

Description automatically generated

1. **Twisted Ring Counter –** It is also known as a switch-tail ring counter, walking ring counter, or Johnson counter. It connects the complement of the output of the last shift register to the input of the first register and circulates a stream of ones followed by zeros around the ring.

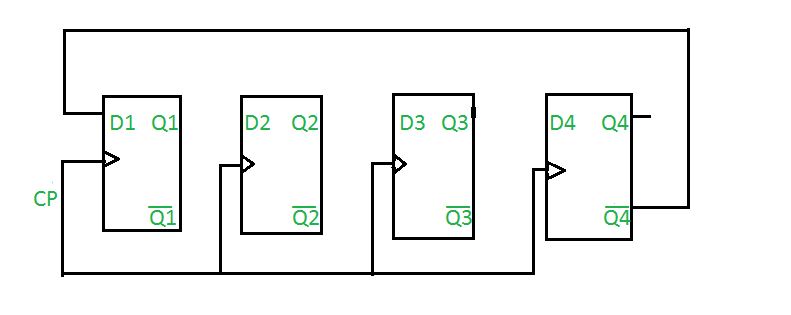
A diagram of a computer circuit

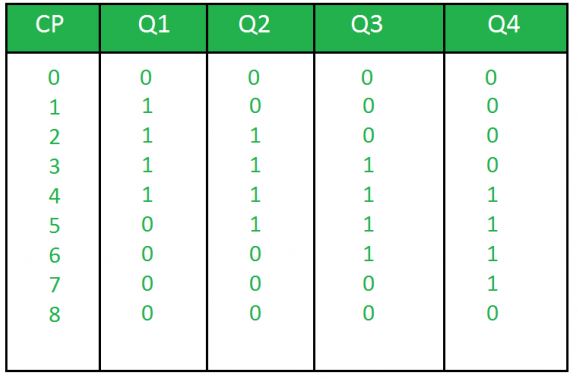
Description automatically generated

1. 4-bit Johnson counter

A Johnson counter is a type of a synchronous counter with a special counting pattern in this case being Johnson counter. It operates by the complemented output of the last flip flop feed back into the input of the first[flip flop](https://www.geeksforgeeks.org/flip-flop-types-their-conversion-and-applications/). What results from this setup is a series of states which forms a sequence that is not characteristic of normal ring [counters](https://www.geeksforgeeks.org/counters-in-digital-logic/).

*Total number of used and unused states in n-bit Johnson counter:   
number of used states=2n   
number of unused states=2n – 2\*n*



TRUTH TABLE:

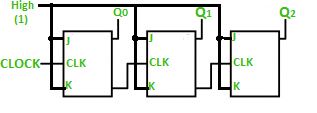
where,   
CP is clock pulse and   
Q1, Q2, Q3, Q4 are the states.

Question: Determine the total number of used and unused states in 4-bit Johnson counter.

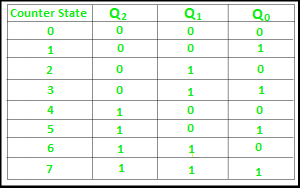
Answer: Total number of used states= 2\*n   
= 2\*4   
= 8   
Total number of unused states= 2n – 2\*n   
= 24-2\*4   
= 8

1. 3-bit Ripple counter

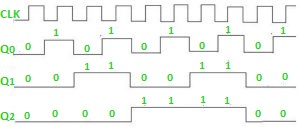
Ripple counter is a cascaded arrangement of flip-flops where the output of one flip-flop drives the clock input of the following flip-flop. A n-bit ripple counter can count up to 2n states. It is also known as MOD n counter.

A 3-bit Ripple counter using a[JK flip-flop](https://www.geeksforgeeks.org/what-is-jk-flip-flop/) is as follows:

Truth Table is as follows:



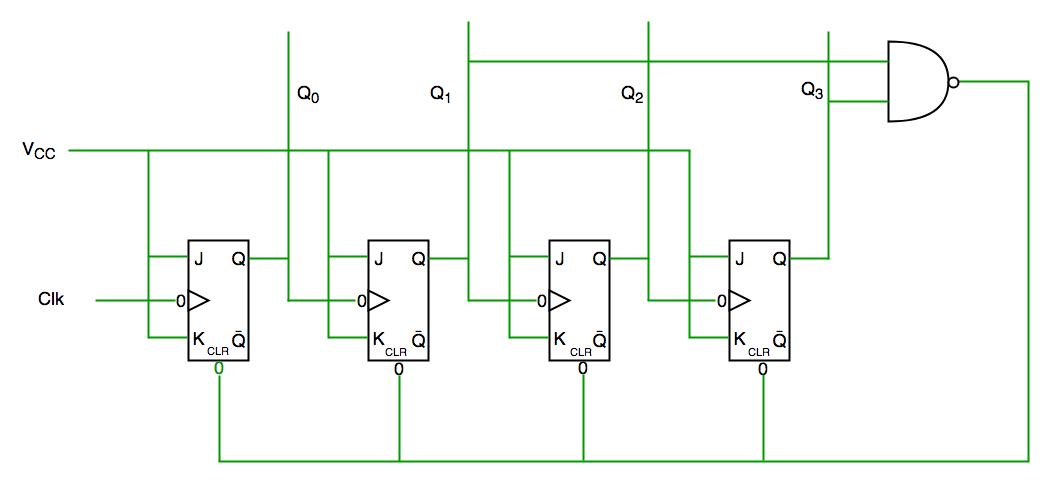
**Timing diagram**



1. Decade Counter

A decade counter counts ten different states and then reset to its initial states. A simple decade counter will count from 0 to 9 but we can also make the decade counters which can go through any ten states between 0 to 15(for 4 bit counter). 

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Clock | Q3 | Q2 | Q1 | Q0 |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 0 | 0 | 0 | 0 |



We see from circuit diagram that we have used nand gate for Q3 and Q1 and feeding this to clear input line because binary representation of 10 is—

1010

And we see Q3 and Q1 are 1 here, if we give NAND of these two bits to clear input then counter will be clear at 10 and again start from beginning.

**Important point**: Number of flip flops used in counter are always greater than equal to (**log2 n**)  where n=number of states in counter.

1. List the difference between:
2. Timers & Counters

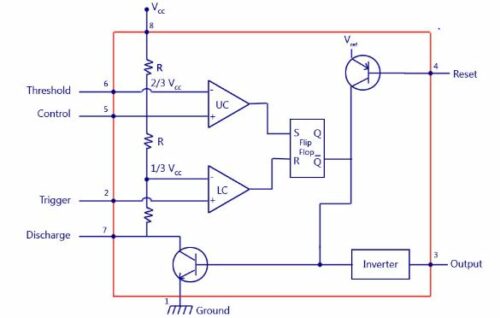
|  |  |
| --- | --- |
| **Timer** | **Counter** |
| The register incremented for every machine cycle. | The register is incremented considering 1 to 0 transition at its corresponding to an external input pin (T0, T1). |
| Maximum count rate is 1/12 of the oscillator frequency. | Maximum count rate is 1/24 of the oscillator frequency. |
| A timer uses the frequency of the internal clock, and generates delay. | A counter uses an external signal to count pulses. |

1. Synchronous & Asynchronous Counters

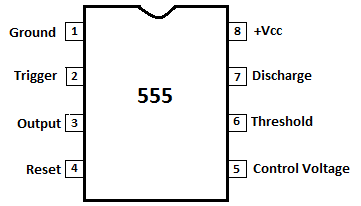
|  |  |  |
| --- | --- | --- |
| **S.NO** | **Synchronous Counter** | **Asynchronous Counter** |
| **1.** | **In synchronous counter we use a universal clock that is common to all flip flops through out the circuit.** | **In asynchronous counter  main clock is only applied to the first flip flop and then for rest of flip flops the output of previous flip flop is taken as a clock.** |
| **2.** | **Synchronous Counter is faster in operation as compared to Asynchronous Counter.** | **Asynchronous Counter is slower as compared to synchronous counter in operation.** |
| **3.** | **Synchronous Counter does not produce any decoding errors.** | **Asynchronous Counter produces decoding error.** |
| **4.** | **Synchronous Counter is also called Parallel Counter.** | **Asynchronous Counter is also called Serial Counter.** |
| **5.** | **Synchronous Counter designing as well implementation are complex due to increasing the number of states.** | **Asynchronous Counter designing as well as implementation is very easy.** |
| **6.** | **Synchronous Counter will operate in any desired count sequence.** | **Asynchronous Counter will operate only in fixed count sequence (UP/DOWN).** |
| **7.** | **Synchronous Counter examples are:**[Ring counter](https://www.geeksforgeeks.org/digital-logic-ring-counter/)**,**[Johnson counter](https://www.geeksforgeeks.org/digital-logic-n-bit-johnson-counter/)**.** | **Asynchronous Counter examples are:**[Ripple](https://www.geeksforgeeks.org/digital-logic-ripple-counter/)**UP counter, Ripple DOWN counter.** |
| **8.** | **In synchronous counter, propagation delay is less.** | **In asynchronous counter, there is high propagation delay.** |

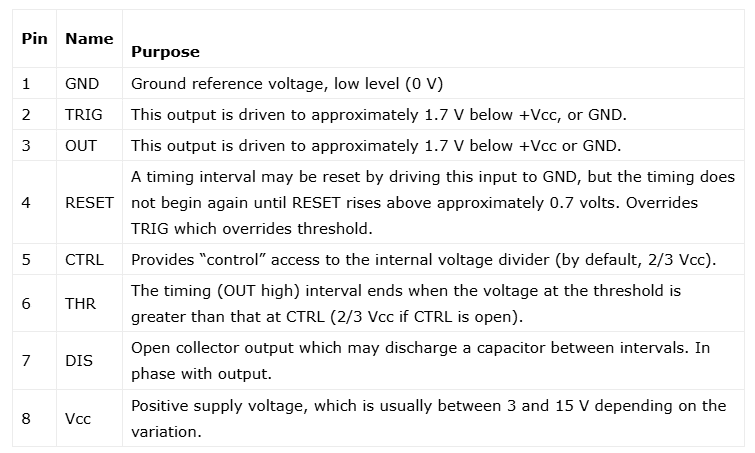
1. Explain working of 555 Timer IC

Ans: The **555 timer IC** is one of the most popular and versatile integrated circuits used in electronics. It operates in three main modes: **Astable**, **Monostable**, and **Bistable**. The 555 timer can be configured to produce time delays, oscillations, or as a flip-flop element.



**555 Time IC Pin Diagram**





**555 Timer Working**

The NE555 timer IC generally operates in 3 modes:

1. Astable Mode
2. Monostable Mode
3. Bi-stable modes

**Astable Mode**

This means there will be no stable level of output. So the output will be swinging between high and low. This character of unstable output is used as a clock or square wave output for many applications.

**Monostable Mode**

This configuration consists of one stable and one unstable state. The stable state can be chosen as either high or low by the user. If the stable output is set at high (1), the output of the timer is high (1).

At the application of an interrupt, the timer output turns low (0). Since the low state is unstable it goes to high (1) automatically after the interrupt passes. Similar is the case for a low stable [monostable mode](https://www.electronicsforu.com/videos-slideshows/setup-555-timer-circuit-monostable-mode).

**Bi-stable Mode**

In bistable mode, both the output states are stable. At each interrupt, the output changes from low (0) to high (1) and vice versa, and stays there. For example, if we have a high (1) output, it will go low(0) once it receives an interrupt and stays low (0) till the next interrupt changes the status.